I. AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Cancelled)

2-45. (Cancelled)

46. (Currently Amended) A transmitter chip comprising:

a divider for receiving a signal and dividing the signal into a first component and a second component;

a first and second channel for receiving the first and second components, respectively, the first and second channels comprising at least one first and second attenuator and a first and second series of phase shifters, respectively;

a quadrature hybrid coupler for outputting a first and second signal based on signals received from the first and second channels;

a first and second 90° phase shifter for receiving the first and second signals from the quadrature hybrid coupler, respectively, and for outputting an RF signal to a cross-polarized radiator element.

47. (Previously Presented) The transmitter chip of claim 46, wherein the divider, the first and second channels, the quadrature hybrid coupler, and the first and second 90° phase shifter are comprised on a single monolithic transmitter chip.

48. (Previously Presented) The transmitter chip of claim 46, the first and second series of phase shifters and first and second attenuators collectively control a scan angle of the RF signal.

49. (Currently Amended) The transmitter chip of claim 46, wherein the first and second series of phase shifters, the at least one first and second attenuators, and the quadrature hybrid coupler collectively control ~~the~~ a linear polarization of the RF signal.

50. (Currently Amended) The transmitter chip of claim 46, wherein the ~~two~~ first and second 90° phase shifters and ~~two~~ first and second attenuators control ~~the~~ a circular polarization angle of the RF signal.

51. (Previously Presented) The transmitter chip of claim 46, wherein the first and second 90° phase shifters control circular polarization of the RF signal.

52. (Currently Amended) The transmitter chip of claim 46, wherein the divider, the first and second channels, the quadrature hybrid coupler, and the first and second 90° phase shifter are comprised on a single monolithic transmitter chip, further comprising a digital serial to parallel converter comprised on the single monolithic transmitter chip.

53. (Previously Presented) The transmitter chip of claim 52, wherein the digital serial to parallel converter controls the first and second attenuators, the first and second series of phase shifters, and the first and second 90° phase shifters.

54. (Previously Presented) The transmitter chip of claim 46, wherein the single monolithic transmitter chip comprises a gallium arsenide transmitter chip.

55. (Previously Presented) The transmitter chip of claim 46, wherein the divider comprises a Wilkinson divider.

56. (Previously Presented) The transmitter chip of claim 46 wherein each of the first and second series of phase shifters comprises a 5.625° phase shifter, an 11.25°

phase shifter, a 22.5° phase shifter, a 45° phase shifter, a 90° phase shifter, and a 180° phase shifter.

57. (Previously Presented) The transmitter chip of claim 46, wherein the first and second series of phase shifters and at least one first and second attenuators comprise a 3-bit attenuator and three single stage amplifiers.

58. (Previously Presented) The transmitter chip of claim 46, wherein transistor-transistor logic (TTL) is used to control the polarization and scan angle of the RF signal.

59. (Previously Presented) The transmitter chip of claim 46, wherein the transmitter chip is capable of generating a signal with a linear polarization angle in the range of about 0° to 90°.

60. (Previously Presented) The transmitter chip of claim 46, wherein the transmitter chip is capable of generating a left-hand and right-hand circularly-polarized RF signal.

61. (Previously Presented) The transmitter chip of claim 46, wherein the transmitter chip is capable of generating a left-hand and right-hand circularly-polarized RF signal with very low axial ratios.

62. (Previously Presented) The transmitter chip of claim 46, wherein the transmitter chip is capable of generating a scan angle in the range of about -45° to 45°.

63. (Previously Presented) The transmitter chip of claim 46, wherein the transmitter chip is manufactured using a multifunction self-aligned gate process (MSAG).

64. (Previously Presented) The transmitter chip of claim 46, wherein the quadrature hybrid coupler comprises a Lange coupler.

65. (Previously Presented) A transmitter chip comprising:

a divider for receiving an RF signal and dividing the RF signal into a first component and second component;

a first and second channel for receiving the first and second components, respectively, the first and second channels comprising at least one first and second attenuator and a first and second series of phase shifters, respectively;

a Lange coupler for outputting two signals based on signals received from the first and second channels;

a first and second 90° phase shifter for receiving a first and second signal from the Lange coupler, respectively, and outputting to a cross-polarized radiator element;

a digital serial to parallel converter for controlling the first and second attenuators, the first and second series of phase shifters, and the first and second 90° phase shifters;

wherein the divider, the first and second channels, the Lange coupler, the first and second 90° phase shifters, and the digital serial to parallel converter are comprised on a single gallium arsenide monolithic transmitter chip.